IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Amended): A semiconductor device comprising:

a semiconductor substrate;

a first insulation layer formed on the semiconductor substrate;

a semiconductor layer insulated from the semiconductor substrate by the insulation layer;

a source region of a first conduction type and a drain region of the first conduction type formed in the semiconductor layer;

a body region of a second conduction type formed in the semiconductor layer between the source region and the drain region, said body region being capable of storing data by accumulating or releasing electric charge;

a second insulation layer formed on the body region;

a word line formed on the second insulation layer and insulated from the body region by the second insulation layer; and

a bit line electrically connected to the drain region,

wherein the area of the body region in contact with the first insulation layer is larger than the area ~~thereof~~ of the body region in contact with the second insulation layer in a cross section along an extending direction of the word line.

Claims 2-3 (Previously Canceled).

Claim 4 (Original): The semiconductor device according to claim 1, wherein the first insulation layer has a thickness equal to or less than five times the thickness of the second insulation layer.

Claim 5 (Previously Canceled).

Claim 6 (Original): The semiconductor device according to claim 1, wherein the body region has a thickness equal to or less than three times the thickness of the first insulation layer.

Claim 7 (Previously Canceled).

Claim 8 (Original): The semiconductor device according to claim 1 further comprising:

a DRAM region including a DRAM having the body region as a part of a memory cell;

a peripheral logic circuit formed around the DRAM region.

Claim 9 (Amended): The semiconductor device according to claim 8, wherein a transistor used in the peripheral logic circuit includes:

a source region of the first conduction type and a drain region of the first conduction type both formed in the semiconductor layer;

a body region of the second conduction type formed between the source region and the drain region in the semiconductor layer;

a third insulation layer formed on the body region; and

a gate electrode formed on the third insulation layer and insulated from the body region by the third insulation layer, and

wherein the area of the body region in contact with the first insulation layer is approximately equal to the area thereof in contact with the third insulation layer when viewed in a cross section along an extending direction of the gate electrode.

Claim 10 (Original): The semiconductor device according to claim 8, wherein the impurity concentration at the interface between the semiconductor substrate and the first insulation layer in the DRAM region is higher than the impurity concentration at the interface between the semiconductor substrate and the first insulation layer in the peripheral logic circuit region.

Claim 11 (Canceled).

Claim 12 (Amended): The semiconductor device according to claim [[11]] 1, wherein the body region has steps on side surfaces thereof in a cross section ~~thereof~~ along an extending direction of the word line.

Claim 13 (Withdrawn): A method of manufacturing a semiconductor device, comprising:

preparing a SOI substrate having a semiconductor layer insulated from a support substrate by a first insulation layer;

forming a mask material on the semiconductor layer;

patterning the mask material;

etching the semiconductor layer in accordance with the mask material and thereby partly exposing the first insulation layer;

implanting an impurity into the support substrate in an energy level permitting the impurity to penetrate the exposed part of the first insulation layer but not permitting same to penetrate the mask material;

forming a third insulation layer between adjacent portions of the semiconductor layer;

removing the mask material;

forming a gate insulating layer on the semiconductor layer;

forming a gate electrode on the gate insulating layer; and

forming a source region and a drain region in the portions of the semiconductor layer at opposite sides of the gate electrode.

Claim 14 (Withdrawn): A method of manufacturing a semiconductor device, comprising:

preparing a SOI substrate having a semiconductor layer insulated from a support substrate by a first insulation layer;

forming a mask material on the semiconductor layer;

patterning the mask material;

etching an upper lying part of the semiconductor layer in accordance with the mask material while maintaining the remainder lower part of the semiconductor layer;

forming a spacer on side surfaces of the mask material and on side surfaces of the upper lying part of the semiconductor layer;

etching the semiconductor layer by using the mask material and the spacer as a mask, and thereby partly exposing the first insulation layer;

forming a third insulation layer between adjacent portions of the semiconductor layer;

removing the mask material;

forming a gate insulating layer on the semiconductor layer;

forming a gate electrode on the gate insulating layer; and

forming a source region and a drain region in the portions of the semiconductor layer at opposite sides of the gate electrode.

Claim 15 (Withdrawn): The method according to claim 14 further comprising:

after the second etching of the semiconductor layer, injecting an impurity into the support substrate in an energy level permitting the impurity to penetrate the exposed part of the first insulation layer but not permitting same to penetrate the mask material.

Claim 16 (Withdrawn): The method according to claim 14 further comprising:

after the first etching of the semiconductor layer, etching part of the semiconductor layer adjacent to the drain region in accordance with the mask material.

Claim 17 (Withdrawn): The method according to claim 14, wherein the body region is used as a part of a memory cell in a DRAM region, and wherein the semiconductor layer is etched in accordance with the mask material without forming the spacer in a peripheral logic circuit region formed around the DRAM region.